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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicants: Bechtolsheim, Frazier, Edsall

Title: Multi-Function High Speed Interface

INFORMATION DISCLOSURE STATEMENT

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Pursuant to 37 CFR 1.97(c), the following information is

submitted for consideration by the examiner:

U.S. Patent #5,570,356

20 Inventor: Finney et al

Title: High Bandwidth Communications System having Multiple

Serial Links.

Issued: Oct 29, 1996

Filed: Jun 7, 1995

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This patent discloses a transmitter 104 which splits

data into a plurality of byte lanes 106, 108, 110, each of

which is 8B/10B encoded and serialized 116, 118, 120, and

then deserialized 136, 138, 140, 10B/8B decoded 146, 148,

5   150 and byte synchronized 152 (col 3 lines 31-54).

U.S. Patent #5,587,709

Inventor: Jeong

Title: High Speed Serial Link for Fully Duplexed Data

10   Communication

Issued: Dec 24, 1996

Filed: Dec. 29, 1995

A serial receiver has a multi-phase oversampled clock

which frames received data by determining clock and data

15   boundaries (col 2 lines 23-26).

U.S. Patent #5,675,584

Inventor: Jeong

Title: High Speed Serial Link for Fully Duplexed Data

20   Communication

Issued: Oct. 7, 1997

Filed: Dec. 29, 1995

A transmitter related to the receiver of #5,587,709

25   above includes a parallel to serial converter utilizing and

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gates instead of high speed registers (col 8 line 58 to col

9 line 5).

U.S. Patent #5,566,193

 5   Inventor: Cloonan

Title: Method and Apparatus for Detecting and Preventing the

Communication of Bit Errors on a High Performance Serial

Data Link.

Issued: Oct. 15, 1996

10   Filed: Dec 30, 1994

This patent describes an error correction scheme using

a parity generator 46, two fully operational and redundant

links 36o and 38o, and a voting scheme at the receiver 100

which selects an error-free output from the two available

15   outputs.

U.S. Patent #5,864,303

Inventor: Ofek

Title: Encoder/Decoder system and methodology utilizing

20   conservative coding with block delimiters, for serial

communication.

Issued: Sep. 5, 1989

Filed: Feb 13, 1987

This patent describes a methodology for selecting codes

25   for parallel to serial encoding and decoding

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U.S. Patent #4,958,344

Inventor: Scott

Title: System for Transmitting and Receiving Asynchronous

Non-Homogeneous Variable Width Parallel Data over a

Synchronous High Speed Serial Transmission Media.

Issued: Sep. 18, 1990

Filed: May 23, 1989

This patent describes a scalable transmitter 501 and

scalable receiver 1535 coupled via a single serial link 1525

for sending command data 101 and parallel data 102 at

different rates (col 4 lines 24-29).

U.S. Patent #5,625,563

Inventor: Rostoker et al.

Title: Method and System for Reducing the Number of

Connections between a plurality of Semiconductor Devices.

Issued: Apr. 29, 1997

Filed: Jan 9, 1995

A plurality of serial links may be individually enabled

to facilitate device to device communications.

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Respectfully Submitted,

Jay Chesavage

Registration No. 39,137

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